

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Prior Application: T. SAKATA et al
Serial No. 09/349,761
Filed: July 9, 1999

Group Art Unit: 2133
Examiner: J. Torres
For: SEMICONDUCTOR INTEGRATED CIRCUIT
WITH MEMORY REDUNDANCY CIRCUIT

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

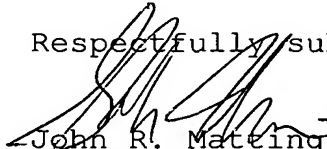
Sir:

In accordance with the duty of disclosure, the applicants inform the Examiner of the documents cited during prosecution of the parent application, Serial No. 09/349,761.

The above-referenced patent application is a continuation application of U.S. Serial No. 09/349,761, filed July 9, 1999, from which priority is claimed under 35 U.S.C. § 120.

Applicants request the Examiner to initial and return a copy of the attached PTO-1449 form to indicate that the references have been considered.

Respectfully submitted,


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Attorney for Applicant(s)

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Date: June 23, 2003

FORM PTO-1449 (REV. 7-80)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. H-780-02	SERIAL NO.		
LIST OF DOCUMENTS CITED BY APPLICANT <i>(Use several sheets if necessary)</i>				APPLICANT T. SAKATA et al			
				FILING DATE		GROUP 2133	
U.S. PATENT DOCUMENTS							
* EXAMINER INITIAL	DOCUMENT	DATE	NAME	CLASS	SUBCLASS	FILING DATE <i>(If Appropriate)</i>	
AA	5,621,691	04/15/97	Park				
AB	5,631,862	05/20/97	Cutter et al				
AC	5,430,679	07/04/95	Hiltebeitel et al				
AD	5,265,055	11/23/93	Horiguchi et al				
AE	4,310,901	01/1982	Harding et al				
AF	6,249,850	06/2001	Kato				
AG	6,119,251	09/2000	Cloud et al				
AH	6,011,734	01/2000	Pappert				
AI	5,841,711	11/1998	Watanabe				
AJ	5,835,504	11/1998	Balkin et al				
AK	6,115,828	09/2000	Tsutsumi et al				
FOREIGN PATENT DOCUMENTS							
	DOCUMENT	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATIO YES NO	
AL	8-77791	03/22/96	Japanese Laid-Open Patent			<input type="checkbox"/>	<input type="checkbox"/>
AM	2-192100	07/27/90	Japanese Laid-Open Patent			<input type="checkbox"/>	<input type="checkbox"/>
AN	4-274096	09/30/92	Japanese Laid-Open Patent			<input type="checkbox"/>	<input type="checkbox"/>
AO						<input type="checkbox"/>	<input type="checkbox"/>
AP						<input type="checkbox"/>	<input type="checkbox"/>
OTHER DOCUMENTS <i>(Including Author, Title, Date, Pertinent Pages, etc.)</i>							
	AR	IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. 28, No. 11, Nov. 1993, "256-Mb					
		DRAM Circuit Technologies for File Applications", G. Kitsukawa et al, pp. 1105-1113.					
	AS						
	AT						
EXAMINER				DATE CONSIDERED			
<small>* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form next communication to applicant.</small>							

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* EXAMINER INITIAL	DOCUMENT	DATE	NAME	CLASS	SUBCLASS	FILING DATE <i>(If Appropriate)</i>
	AA	6,052,798	04/2000	Jeddeloh		
	AB	6,026,505	02/2000	Hedberg et al		
	AC	6,018,811	01/2000	Merritt		
	AD	6,011,733	01/2000	Fischer et al		
	AE	5,983,374	11/1999	Todome et al		
	AF	5,920,515	07/1999	Shaik et al		
	AG	5,917,764	06/1999	Ohsawa et al		
	AH	5,909,404	06/1999	Schwarz		
	AI	5,859,804	01/1999	Hedberg et al		
	AJ	5,841,710	11/1998	Larsen		
	AK	5,831,989	11/1998	Fujisaki		

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OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, etc.)*

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* EXAMINER INITIAL		DOCUMENT	DATE	NAME	CLASS	SUBCLASS	FILING DATE <i>(If Appropriate)</i>
	AA	5,808,944	09/1998	Yoshitake et al			
	AB	5,699,306	12/1997	Lee et al			
	AC	5,684,746	11/1997	Oowaki et al			
	AD	5,644,541	07/1997	Siu et al			
	AE	5,640,353	06/1997	Ju			
	AF	5,485,424	01/1996	Kawamura			
	AG	4,876,685	10/1989	Rich			
	AH	4,475,194	10/1984	LaVallee et al			
	AI	5,471,427	11/1995	Murakami et al			
	AJ	5,487,039	01/1996	Sukegawa			
	AK	5,933,376	08/1999	Lee			
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